Ronan BARZIC
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47 years old, French, married, 2 children

IEEE and ACM member

Experienced Digital IC Designer Engineer

Strong experience in low power microcontroller design

WORK EXPERIENCES

Since Sep. 11 ***Atmel Norway AS :*** **Staff IC design Engineer. maXTouch IC design team**
maXTouch T & U-serie AVR32 touchscreen controller design
- Power/clock/reset manager design, verification and silicon validation (mXT874U)
- System level RTL design and verification
- various R&D activities, including test chips, FPGA and PCB design
- Training/Mentoring
- Chip specifications

Jan 06-Sept 11 ***Atmel Norway AS:*** **Senior Discipline Manager, Mid-end – AVR32 design Team**
AVR32-based application processor and microcontroller development.
- Power management
- Analog integration
- Design Flow (common ARM/AVR32 platform)

Mar 01–Dec 05 ***Atmel Nantes SA (France):*** **Senior IC design Engineer.**
Microcontroller IC design team
C251, 8-bit AVR & AVR32 microcontroller design

Jan 00–Jan 01 ***Alcatel Mobile Phone Division (France):*** **Senior R&D Engineer**
Development of OneTouch 50x and 70x mobile phones

Oct 95–Dec 99 ***Visio Nerf (France) :*** **Senior R&D Engineer**
Development of several computer-assisted vision systems (hardware and software)

Oct 92 –Oct 95 ***INRIA/France Telecom (France) :*** **Research team member**
Development of a SIMD video processor

EDUCATION

1990-1991 **Postgraduate degree (Master equivalent) in MicroElectronic - with Honor**
Institut National Polytechnique de Grenoble (INPG) France
Scholarship from French and Québec governments: 9 month stay in Sherbrooke University (Québec/Canada)

1987-1991 **Engineering Degree in Electronic**
Ecole Supérieure d'Èlectronique de l'Ouest (ESEO) France

Languages **Norwegian** : beginner **English** : fluent
French : mother tongue

Programming languages: Verilog, SystemVerilog, C/C++, Python,Perl,Prolog, Clojure, Scala

LEISURES

Sports: Swimming, squash, surf
RC planes, astronomy
Electronic and computers (Arduino, Free & Open Source Softwares…)

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Additional details about professional experiences

Staff Design Engineer - mXT Design Team - Atmel Norway (Present)

- ***Development of a new power/clock/reset management system, including retention flipflops support , back-biasing control and event-based power/clock gating control***
  - Pre-studies/Specifications/Presentations to management
  - RTL design + UPF / Verilog & C Code generators / C API
  - Integration in actual devices
  - Pre/post-layout verification, asynchronous assertions
  - Silicon validation framework development (stress testing)
  - Trainings (for Design, Test and Application teams)

- ***R&D activities***
  - Test chips (from RTL to layout), using Design Compiler,Encounter and Virtuoso
  - FPGA prototyping (daughter board PCB design, PC interfacing using Python/Qt)
  - Student project mentoring (asynchronous design, CPU design, GALS systems)

- ***Support project and team managers regarding detailed product specifications***
  Focus on:
  - Interaction of various subsystems like I2C, USB, touch controller with the power & clock management subsystem
  - Power consumption targets, power domain definitions

Senior Discipline Manager, AVR32 Midend - AVR32 Design Team - Atmel Norway

- ***Member of the first AP7 (AVR32-based application processor) and first UC3 (AVR32-based flash microcontroller) design team***
  - power & clock management system, analog integration, pad ring definition
  - RTL design and verification (IP level and system level)
  - Design flow improvements (scripting)
  - Development of a mixed-signal simulation flow (RTL+Spice+Verilog-AMS) and a full-chip Spice simulation flow (Nanosim)
  - Development of tools to help checking correct integration of analog cells (Perl + Prolog)
- Development of a common AVR32/ARM (Cortex M0+/Cortex M4) design platform (together with Atmel Nantes design team)
  - Flow and methodology alignment

- Contribution to the design of the SAM4L4 circuit (RTL verification, full-chip Spice simulation)

Senior Design Engineer, Atmel Nantes (France)

- ***8-bit microcontrollers***
  - C251 "redesign" (conversion of 2-phase design to a single clock design)
  - AT90CAN128 (AVR microcontroller with CAN bus interface)
    - RTL database transfer and verification (3 months stay in Norway)
    - FPGA design for In-Circuit Emulator platform
    - introduction of static timing analysis using PrimeTime
  - AT90PWM2/3 (AVR microcontroller with dedicated lightning/motor control hardware)
    - Design leader (design team : 5 engineers)
    - Introduction of formal verification (Formality)
- ***32-bit microcontroller***
  - First collaboration with Atmel Norway AVR32 team
  - Place and route of the AVR32 chip

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Senior R&D Engineer, Alcatel Mobile Phone - France (Jan 2000 - Jan 2001)

- ***One Touch 300/500 mobile phone integration***
  - Prototype validation – Focus on the audio subsystem

Senior R&D Engineer, Visio Nerf - France (Oct 95 - Dec 99)

- ***Development of computer-assisted industrial vision system***
  - Board design (Schematic+PCB)
  - FPGA design
  - Firmware development on Transputer and TI C6x (RTOS porting, drivers)
  - Prototype debugging
  - Production support
  - Customer support (off & on-site)

Research Team Member – INRIA/France Telecom - France (Oct 92 - Sept 95)

- ***Research project on massively parallel architecture for video compression - in charge of the CPU specification***
  - VHDL development (Compass)
  - SIMD simulator development (C++)
  - Fractal compression algorithm development (C)

Postgraduate training period - Sherbrooke University (Jan 91 - Jun 91)

- ***Development of a CMOS voltage reference using a floating gate transistor***
  - Full-custom analog design on a multi-wafer project (Spice, Cadence)